UNITED STAT DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/394,564	09/10/99	OLNOWICH	H EN997080B

EXAMINER	
BATAILLE, P	8

TM21/0907

SHELLEY M BECKSTRAND PC
ATTORNEY AT LAW
314 MAIN STREET
OWEGO NY 13827

ART UNIT: 2186

DATE MAILED: 09/07/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)

1- File Copy

Advisory Action

Application No.	Applicant(s)
09/394,564	Howard T Olnowich
Examiner	**Group Art Unit**
P. Bataille	2186

THE PERIOD FOR RESPONSE: [check only a) or b)]

a) ☒ expires 3 months from the mailing date of the final rejection.

b) ☐ expires either three months from the mailing date of the final rejection, or on the mailing date of this Advisory Action, whichever is later. In no event, however, will the statutory period for the response expire later than six months from the date of the final rejection.

Any extension of time must be obtained by filing a petition under 37 CFR 1.136(a), the proposed response and the appropriate fee. The date on which the response, the petition, and the fee have been filed is the date of the response and also the date for the purposes of determining the period of extension and the corresponding amount of the fee. Any extension fee pursuant to 37 CFR 1.17 will be calculated from the date of the originally set shortened statutory period for response or as set forth in b) above.

☐ Appellant's Brief is due two months from the date of the Notice of Appeal filed on _____ (or within any period for response set forth above, whichever is later). See 37 CFR 1.191(d) and 37 CFR 1.192(a).

Applicant's response to the final rejection, filed on *Aug 24, 2001* **has been considered with the following effect, but is NOT deemed to place the application in condition for allowance:**

☐ The proposed amendment(s):

☐ will be entered upon filing of a Notice of Appeal and an Appeal Brief.

☐ will not be entered because:

☐ they raise new issues that would require further consideration and/or search. (See note below).

☐ they raise the issue of new matter. (See note below).

☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal.

☐ they present additional claims without cancelling a corresponding number of finally rejected claims.

NOTE: _____

☐ Applicant's response has overcome the following rejection(s):

_____

☐ Newly proposed or amended claims _____ would be allowable if submitted in a separate, timely filed amendment cancelling the non-allowable claims.

☒ The affidavit, exhibit or request for reconsideration has been considered but does NOT place the application in condition for allowance because:
the claims do not recite any features which would estblish the difference between the system by Hagersten US5,860,109 and Gupta (US5,535,116), see attachment.

☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

☒ For purposes of Appeal, the status of the claims is as follows (see attached written explanation, if any):

Claims allowed: *none*

Claims objected to: *none*

Claims rejected: *1 and 31-39*

☐ The proposed drawing correction filed on _____ ☐ has ☐ has not been approved by the Examiner.

☐ Note the attached Information Disclosure Statement(s), PTO-1449, Paper No(s). _____ .

☐ Other

ADVISORY ACTION

Response to Arguments

1. Applicant's arguments, with respect to the claims rejected under 35 U.S.C. 103 over Gupta et al. (US5,535,116) in view of Hagersten et al. (US5,860,109), have been fully considered but are not deemed to be persuasive for at least the following.

Applicant argues that neither reference teaches " each processing node including a unique section of shared memory which is not cache and an adapter for storing changed data to each unique section so that each section contains the most recent data. Unlike applicant's remarks, Hagersten clearly teach a plurality of processing nodes [12, Fig. 1] interconnected through interconnecting network [14, Fig. 1]; each processing node including multiple processors (32A-D), multiple cache memories (34-A-D) and local memory (36A-D), all local memories or memory portions of the processing nodes collectively form a distributive shared memory which may be accessed in non-uniform memory architecture (NUMA) fashion, i.e. each of said multi-processing nodes includes an addressable portion or local memory modules of the global system memory or sub-divided portion of the global physical system memory [Col. 9, Lines 31-53; Col. 8, Lines 53-67]; and each processing node having said local memory is capable of storing valid and shared copies of requested ones of data signals stored in the main memory modules [Col. 6, Lines 36-42; Col. 9, Line 1-13; Col. 13, Lines 21-45].

In contrast to applicant's assertion, Hagersten in many instances indicates that each node of the plurality of nodes shares a shared distributed memory wherein sections or addressable loccations of the shared distributed memory are accessible to more than one of the processing nodes [Col. 6, Lines 36-42; Col. 13, Line 1-8; Col. 14, Lines 28-45].

Hagersten's system does not simply provides bus operations, as argued by applicant, but provides a coherency system maintaining coherency between the memories within the multi-processing nodes communicated via an interconnecting network (14, Fig. 1; 38 and 48, Fig. 1 and 2) [Col. 9, Line 30; Col. 10, Line 5].

The applicant is right regarding Hagersten having "external device owning exclusive copy can unilaterally modify the copy without having to inform other entities". However, this is for an inter-node or processor-bus transaction within a subnode since all processors within a node have respective cache memory, but common local memory or system memory portion. Hagersten's system maintains internode coherency detecting addresses which require data transfer to or from another processing node, i.e. accessed addresses within the address space of a node corresponding to addresses within locations of another processing are maintained in such a way to maintain consistency such that modified copies of data are written through so that all nodes maintaining a shared copy are allowed to cache the most current copy of a modified memory block [Col. 9, lines 1-14; Col. 10, Lines 1-27; Col. 16, Lines 18-28; Col. 18, Line 62 to Col. 19, Line 14; Col. 19, Lines 32-40; Col. 16, Lines 35-42].

Contact Information

2. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 305-9731.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tuesday to Friday from 7:30 P.M. to 6:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim, can be reached on (703) 305-3821. The fax phone number for this Group is (703) 308-9731.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

P.B.

P. Bataille

September 6, 2001

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100